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Performance Evaluation of Synchronization of Chua's System Under Different Memductance

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Abstract: Practical implementation of synchronization schemes is important for secure communication. With many systems available, simple systems with varying differences will prove pertinent in user identification and inter-operability of communicating units. The implementation of Chua's circuit with different memristors is a potential candidate for the realization of such units. In this paper, a general control function for the synchronization of two Chua's circuits with similar or dissimilar memristors was developed. Three different memristor circuits were considered in this paper. Numerical simulation of the proposed control function was carried out and the performance of different memristors in the similar and dissimilar configuration was considered.

Keywords: *memristor; active control; Chua's circuit; synchronization.*

Mathematics Subject Classification (2010): 34H10, 93C10.

1 Introduction

The application of chaotic systems in secure communications has led to the development of several synchronization schemes. Initially, synchronization of chaotic systems was between two identical systems [1] before it was extended from two different chaotic systems to the increased and reduced order synchronization between two systems [2], increased and reduced order between three or more systems [3, 4], synchronization of fractional order systems [5], delay differential equations, discrete chaotic systems, and electronic realization [6].

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Different types of synchronization such as complete synchronization, lag synchronization, generalized synchronization, projective synchronization, and function projective synchronization have been developed. There exist several synchronization techniques including the active control, backstepping, Open-Plus-Closed-Loop (OPCL), recursive active control. Studies have shown that the active control method has better performance for integer order [7] and fractional order systems [5].

Implementation of synchronization is required for real time applications in secure communication. Electronic circuit design and implementation of chaotic systems are important in the understanding of dynamic systems and practical implementation. The discovery of chaos in electronic circuits by Chua [8] initiated a new line of research [9]. Chua's chaotic circuit has been extensively studied with several modifications. Combination synchronization of memristive circuit was realized through the diffusive and negative feedback coupling [6], time delayed sliding mode synchronization in a novel chaotic memcapacitor [10], design of low dimensional fractional order nonautonomous system based on the Chua system [11], experimental realization of synchronization in a network using Chua's circuit [12].

The main goal of this paper is to investigate the behaviour of different memristors under synchronization using an active control method. The performance of different memristors is important in real life implementation of synchronization for secure communication. Hence, the speed of synchronization and fluctuations before synchronization are considered in this paper. In Section 2, the system and different memristors to be considered are discovered while the synchronization of the systems is discussed in Section 3. Results are presented in Section 4 and conclusions are given in Section 5.

2 System Description

Chua's circuit is given by the expression [13]

$$\begin{aligned} \dot{x} &= \alpha(y - f(x)), \\ \dot{y} &= x - y + z, \\ \dot{z} &= -\beta y, \end{aligned} \tag{1}$$

where x, y, z are state space of the system, and the piecewise linear function $f(x)$ is defined as

$$f(x) = \begin{cases} \alpha(y - bx - (b - a), & \text{if } x < -1; \\ \alpha(y - ax), & \text{if } -1 \leq x \leq 1; \\ \alpha(y - bx - (a - b)), & \text{if } x > 1, \end{cases}$$

a, b, c are constants.

By replacing Chua's diode with a flux controlled memristor, Itoh and Chua [14] transformed the canonical Chua circuit into a 4 D system of the form

$$\begin{aligned} \dot{y}_1 &= \frac{1}{C_1 R}(y_2 - y_1) - \frac{1}{C_1} y_1 W_i, \\ \dot{y}_2 &= \frac{1}{C_2 R}(y_1 - y_2) - y_3, \\ \dot{y}_3 &= \frac{1}{L} y_2 - \frac{r}{L} y_3, \\ \dot{y}_4 &= y_1, \end{aligned} \tag{2}$$

where C_1, C_2, L are the circuit elements and W_i is the memductance. In this paper, the synchronization of system (2) will be investigated under three different flux controlled memristors.

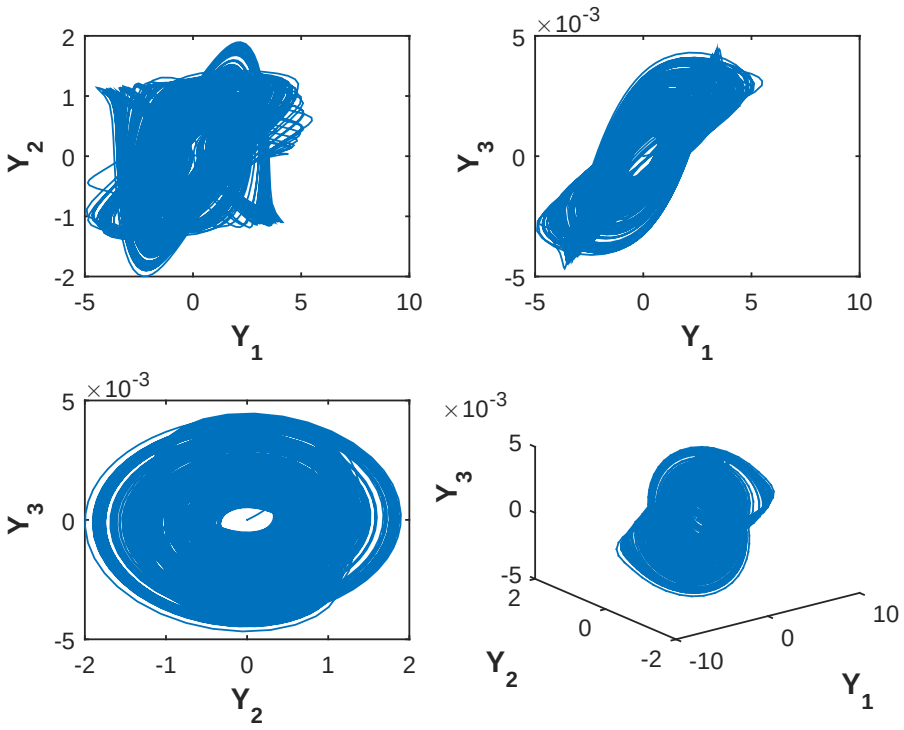

Figure 1: Phase space realization of Chua's circuit with a memristor of the form $W_i = -a+b|y_4|$, where the values of a and b are taken as 0.6667×10^{-3} and 1.4828, respectively.

2.1 Memristor of type I

By replacing Chua's diode in Chua's chaotic circuit with an active flux memristor, a new memristor based chaotic circuit was obtained by [15] as

$$\begin{aligned} \dot{x} &= \alpha(y - x - W(w)x), \\ \dot{y} &= x - y + z, \\ \dot{z} &= -\beta y - \gamma z, \\ \dot{w} &= x, \end{aligned} \tag{3}$$

where $W(w) = -a + b|w|$. The system was found chaotic for a wide range of values of $|w|$. The circuit form was given and implemented by [16] as

$$\begin{aligned}
\frac{dv_1}{dt} &= \frac{1}{C_1}\left(\frac{v_2 - v_1}{R} - W(\phi)v_1\right),\\
\frac{dv_2}{dt} &= \frac{1}{C_2}\left(\frac{v_1 - v_2}{R} - i_3\right),\\
\frac{di_3}{dt} &= \frac{1}{L}(v_2 - v_1),\\
\frac{d\phi}{dt} &= v_1.
\end{aligned} \tag{4}$$

The phase space representation of this system is shown in Figure 1.

2.2 Memristor of type II

A memductance function of the form

$$W(\phi) = \frac{dq(\phi(t)}{d\phi(t)} = -a + 3b\phi^2(t) \tag{5}$$

was introduced to extend 4D chaotic Chua's circuit proposed in [17] to a 5D system by [18]. The proposed systems thus became

$$\begin{aligned}
\frac{dx_1(t)}{dt} &= \frac{1}{C_1}(x_3(t) - W(x_5(t))x_1(t),\\
\frac{dx_2(t)}{dt} &= \frac{1}{C_2}(-x_3(t) + x_4(t)),\\
\frac{dx_3(t)}{dt} &= \frac{1}{L}(x_2(t) - x_1(t) - Rx_3(t)),\\
\frac{dx_4(t)}{dt} &= \frac{-x_2(t)}{L_2},\\
\frac{dx_5(t)}{dt} &= x_1(t).
\end{aligned} \tag{6}$$

The system was reported to exhibit chaos for certain system parameters. The phase space and dynamics of equation (2) with memristor of the form (5) is presented in Figure 2.

2.3 Memristor of type III

A dimensionless flux controlled memristor model with fifth order flux polynomial was proposed by [19] as

$$\begin{aligned}
\dot{x} &= \alpha(y + x - W(w)x),\\
\dot{y} &= \beta x + \gamma y - z,\\
\dot{z} &= \delta y - z,\\
\dot{w} &= x,
\end{aligned} \tag{7}$$

where the memductance $W(\phi)$ is defined as

$$W(\phi) = a\phi^4 - b\phi^2 - c, \tag{8}$$

The phase space and dynamics of equation (2) with memristor of the form (8) is presented in Figure 3.

3 Synchronization

Theorem 1 *If the drive and response systems of the form (2) have the memristive elements given by W_i^j and W_i^k, respectively (where $i = 1, 2, 3$ are the different types of memristors being considered), complete synchronization will be achieved by the method of active control if the control function is chosen as*

$$\begin{aligned} u_1(t) &= \frac{1}{C_1} y_1 W_i^j - \frac{1}{C_1} x_1 W_i^k + \left(\lambda_1 + \frac{1}{C_1 R}\right) e_1 - \frac{1}{C_1 R} e_2, \\ u_2(t) &= \frac{1}{C_2 R} e_1 + \left(\lambda_2 + \frac{1}{C_2 R}\right) e_2 + \frac{1}{C_2} e_3, \\ u_3(t) &= -\frac{1}{L} e_2 + \left(\lambda_3 + \frac{r}{L}\right) e_3, \\ u_4(t) &= e_1 + \lambda_4 e_4, \end{aligned} \tag{9}$$

where λ_i are chosen to be negative and $e_i = y_i - x_i$, then the drive system (2) will achieve multi-switching synchronization with the response system.

Proof. Take equation (2) as the drive system and the following ones as the response system

$$\begin{aligned} \dot{x}_1 &= \frac{1}{C_1 R}(x_2 - x_1) - \frac{1}{C_1} x_1 W_i + u_1(t), \\ \dot{x}_2 &= \frac{1}{C_2 R}(x_1 - x_2) - x_3 + u_2(t), \\ \dot{x}_3 &= \frac{1}{L} x_2 - \frac{r}{L} x_3 + u_3(t), \\ \dot{x}_4 &= x_1 + u_4(t), \end{aligned} \tag{10}$$

where u_i are the controllers to be determined. Substituting equations (2) and (10) into the error dynamics $e_i = y_i - x_i$, where $i = 1, 2, 3$, we obtain

$$\begin{aligned} \dot{e}_1 &= \frac{1}{C_1 R}(e_2 - e_1) - \frac{1}{C_1} y_1 W_i^j + \frac{1}{C_1} x_1 W_i^k + u_1(t), \\ \dot{e}_2 &= \frac{1}{C_2 R}(e_1 - e_2) - e_3 + u_2(t), \\ \dot{e}_3 &= \frac{1}{L} e_2 - \frac{r}{L} e_3 + u_3, \\ \dot{e}_4 &= e_1 + u_4, \end{aligned} \tag{11}$$

To achieve asymptotic stability of system (11), the terms, which are nonlinear in e_i, are eliminated as follows:

$$\begin{aligned} u_1 &= \frac{1}{C_1} y_1 W_i^j - \frac{1}{C_1} x_1 W_i^k + v_1(t), \\ u_2 &= v_2(t), \\ u_3 &= v_3, \\ u_4 &= v_4, \end{aligned} \tag{12}$$

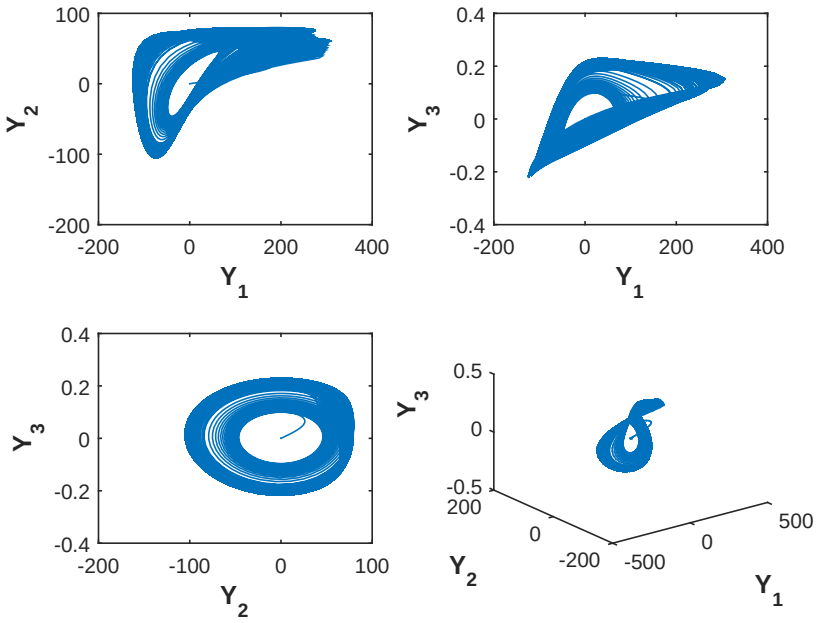

Figure 2: Phase space realization of Chua's circuit with the memristor of the form $W_i = -a + 3by_4^2$, where the values of a and b are taken as 0.6667×10^{-3} and 1.4828, respectively.

substituting (12) into (11) gives

$$\begin{aligned}
\dot{e}_1 &= \frac{1}{C_1 R}(e_2 - e_1) + v_1(t), \\
\dot{e}_2 &= \frac{1}{C_2 R}(e_1 - e_2) - e_3 + v_2(t), \\
\dot{e}_3 &= \frac{1}{L}e_2 - \frac{r}{L}e_3 + v_3, \\
\dot{e}_4 &= e_1 + v_4.
\end{aligned} \tag{13}$$

Using the active control method, a constant matrix $\mathbb{D}$ is chosen which will control the error dynamics (13) such that the feedback matrix is $V_i = \mathbb{D}e_i$. There are various choices of the feedback $\mathbb{D}$ which can be chosen to control the error dynamics [20]. We chose $\mathbb{D}$ to be of the form

$$\mathbb{D} = \begin{pmatrix} \left(\lambda_1 + \frac{1}{C_1 R}\right) & -\frac{1}{C_1 R} & 0 & 0 \\ \frac{1}{C_2 R} & \left(\lambda_2 + \frac{1}{C_2 R}\right) & 1 & 0 \\ 0 & -\frac{1}{L} & \left(\lambda_3 + \frac{r}{L}\right) & 0 \\ 1 & 0 & 0 & \lambda_4 \end{pmatrix}. \tag{14}$$

If the eigenvalues λ_i are chosen to be negative, a stable synchronization between the drive and response system will be achieved.

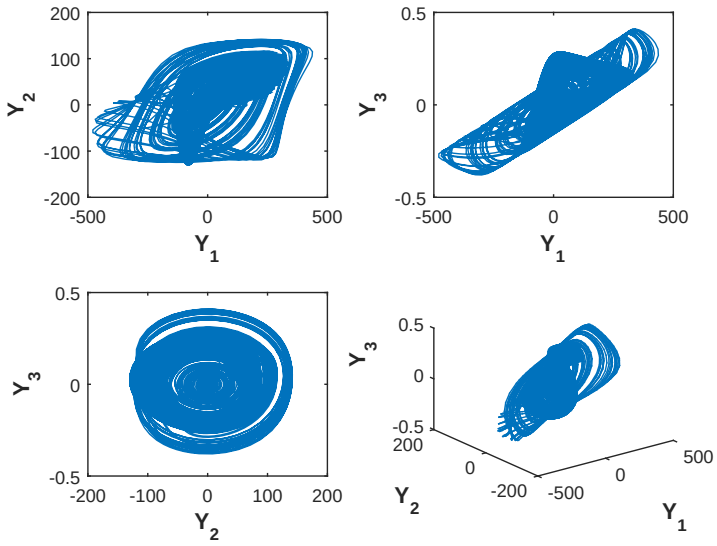

Figure 3: Phase space realization of Chua's circuit with memristor of the form $W_i = ay_4^4 - by_4^2 - c$, where the values of a b and c are taken as 1000, 1.087 and $0.33e^{-3}$, respectively.

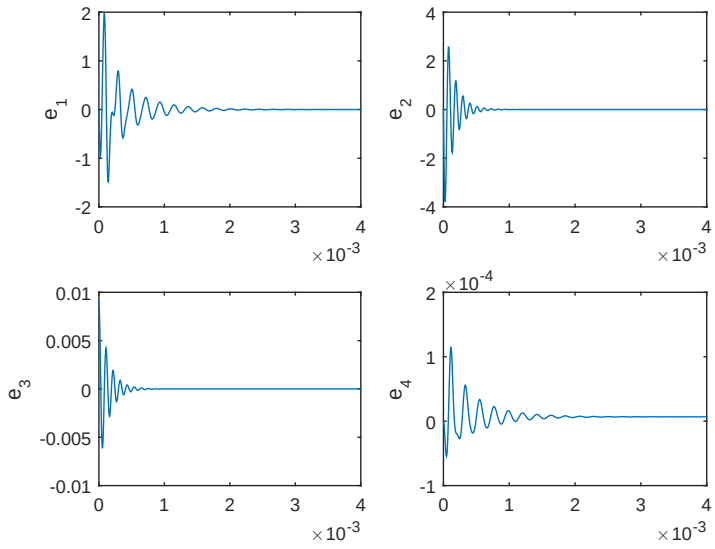

Figure 4: The synchronization error functions for two systems with the memristor of type I using control functions as described in Corollary 3.1.

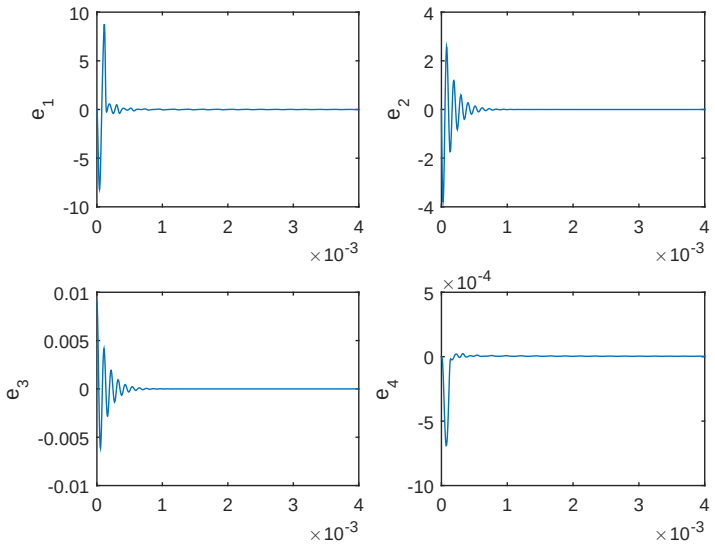

Figure 5: The synchronization error functions for two systems with the memristor of type II using control functions as described in Corollary 3.2.

Corollary 3.1 *If* $W_1^1 = -a_1^1 + b_1^1|y_4|$ *and* $W_1^2 = -a_1^2 + b_1^2|x_4|$, *then the control function (14) can be written as*

$$\begin{aligned} u_1(t) &= \frac{1}{C_1} y_1 W_i^j - \frac{1}{C_1} x_1 W_i^k + \left(\lambda_1 + \frac{1}{C_1 R}\right) e_1 - \frac{1}{C_1 R} e_2, \\ u_2(t) &= \frac{1}{C_2 R} e_1 + \left(\lambda_2 + \frac{1}{C_2 R}\right) e_2 + \frac{1}{C_2} e_3, \\ u_3(t) &= -\frac{1}{L} e_2 + \left(\lambda_3 + \frac{r}{L}\right) e_3, \\ u_4(t) &= e_1 + \lambda_4 e_4. \end{aligned} \tag{15}$$

Corollary 3.2 *If* $W_2^1 = -a_2^1 + 3b_2^1 y_4^2$ *and* $W_2^2 = -a_2^2 + 3b_2^2 x_4^2$, *then the control function (14) can be written as*

$$\begin{aligned} u_1(t) &= \frac{1}{C_1} y_1 W_i^j - \frac{1}{C_1} x_1 W_i^k + \left(\lambda_1 + \frac{1}{C_1 R}\right) e_1 - \frac{1}{C_1 R} e_2, \\ u_2(t) &= \frac{1}{C_2 R} e_1 + \left(\lambda_2 + \frac{1}{C_2 R}\right) e_2 + \frac{1}{C_2} e_3, \\ u_3(t) &= -\frac{1}{L} e_2 + \left(\lambda_3 + \frac{r}{L}\right) e_3, \\ u_4(t) &= e_1 + \lambda_4 e_4. \end{aligned} \tag{16}$$

Corollary 3.3 *If* $W_1^1 = a_3^1 y_4^4 - b_3^1 y_4^2 - c_3^1$ *and* $W_1^2 = a_3^2 y_4^4 - b_3^2 y_4^2 - c_3^2$, *then the control*

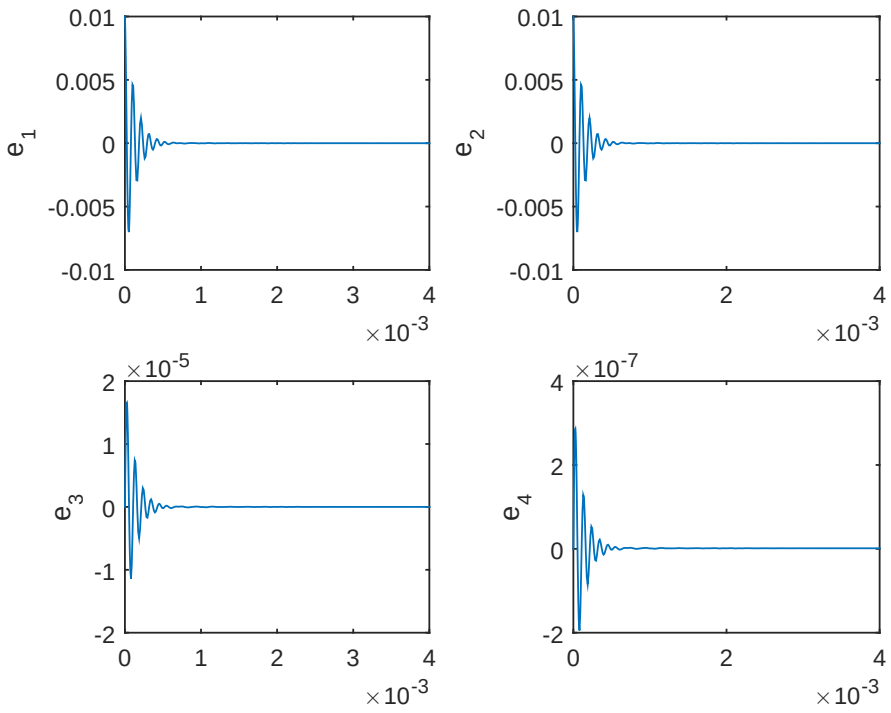

Figure 6: The synchronization error functions for two systems with the memristor of type III using control functions as described in Corollary 3.3.

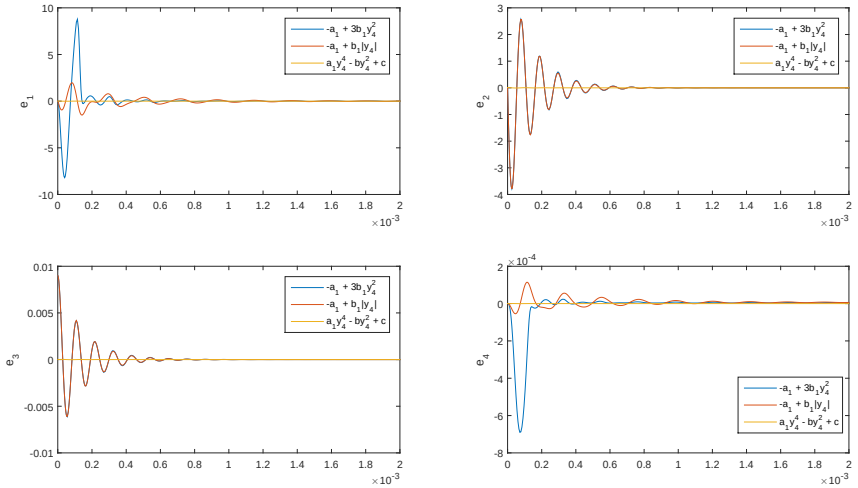

Figure 7: Error functions of different memristors when synchronized with the memristor W_{ii} (where $i = 1, 2, 3$).

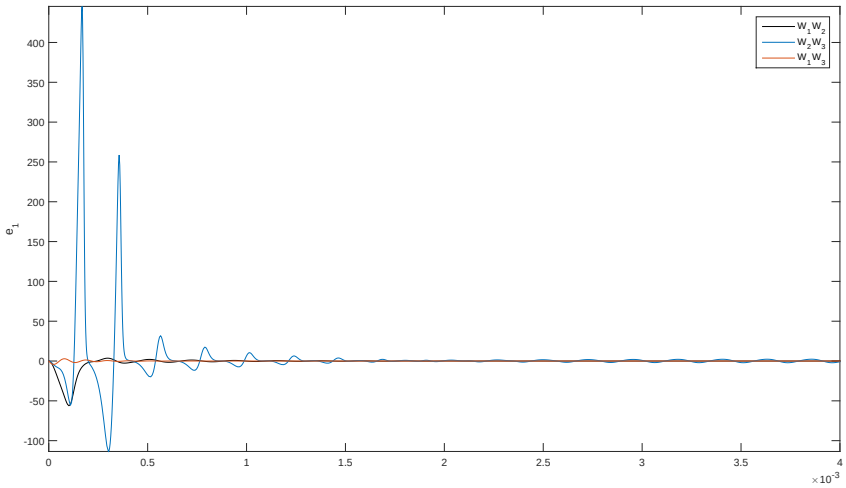

Figure 8: Comparison of the synchronization error for $W_{ij}(i \neq j)$.

function (14) can be written as

$$\begin{aligned} u_1(t) &= \frac{1}{C_1} y_1 W_i^j - \frac{1}{C_1} x_1 W_i^k + \left(\lambda_1 + \frac{1}{C_1 R}\right) e_1 - \frac{1}{C_1 R} e_2, \\ u_2(t) &= \frac{1}{C_2 R} e_1 + \left(\lambda_2 + \frac{1}{C_2 R}\right) e_2 + \frac{1}{C_2} e_3, \\ u_3(t) &= -\frac{1}{L} e_2 + \left(\lambda_3 + \frac{r}{L}\right) e_3, \\ u_4(t) &= e_1 + \lambda_4 e_4. \end{aligned} \tag{17}$$

4 Results

In order to verify the effectiveness of the proposed controllers, numerical simulations were carried out. The system of equations with the proposed controllers was solved using the fourth-order Runge-Kutta method with step size of 0.0001. Using the initial conditions $(y_1, y_2, y_3, y_4) = (10 \times 10^{-3}, 0.02, 0.01, 1 \times 10^{-3})$ and $(x_1, x_2, x_3, x_4) = (9 \times 10^{-3}, 10 \times 10^{-3} 0.0011 \times 10^{-3})$, the controllers described in Corollary 3.1 were implemented. The results are shown in Figure 4. The synchronization errors between the two systems when $W_1 = -a_1 + b_2|y_4|$ and $W_2 = -a_2 + b_2|x_4|$ were simulated. Similarly, the synchronization error between system (2) and (10) when $W_1 = -a_1 + 3b_2 y_4^2$ and $W_2 = -a_2 + b3_2 x_4^2$ using the initial conditions $(y_1, y_2, y_3, y_4) = (10 \times 10^{-3}, 0.02, 0.01, 1 \times 10^{-3})$ and (x_1, x_2, x_3, x_4) $= (9 \times 10^{-3}, 10 \times 10^{-3} 0.0011 \times 10^{-3})$ are simulated and the results are shown in Figure 5. In the same vein, the control functions as described in Corollary 3.3 were simulated using two memristor of type III. The result is shown in Figure 6. The performance of each memristor, when synchronized in the form W_{ii}, can be investigated from Figure 7. The memristor of type II showed the worst performance while the memristor of

type III exhibited the best performance. The error fluctuation were the greatest for the memristor of type II and the lowest for the memristor of type III. In Figure 8, the performance of synchronization of the system under two different memristors $W_{ij}(i \neq j)$ is reported using only the first error component e_1. The combination of W_1W_3 has the lowest fluctuations before synchronization and the fastest synchronization of the three different combinations. The worst performance was the combination W_2W_3 which has the highest fluctuations amongst the three and the slowest convergence.

5 Conclusion

In this paper, we have investigated the synchronization of different memristors in the same circuit with identical and non-identical memristors. Suitable controllers were designed using the method of active control. Numerical simulation results showed that the controllers were effective. The performance of the three memristors was investigated using fluctuations before synchronization and time to synchronization. In the synchronization between two similar memristors, the memristor of type III was found to have the best performance. However, the synchronization of memristors of type I and III exhibited the fastest synchronization and least fluctuation, making it the best performing. This scheme will find application in a multiuser secure communication environment. Further investigation may be carried out on the multi-switching, time delayed and practical implementation of this scheme.

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